UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/919,361	07/30/2001	Steven C. Woo	RB1-026US	2536

44429 7590 12/20/2005

SHEMWELL MAHAMEDI LLP
4880 STEVENS CREEK BOULEVARD, SUITE 201
SAN JOSE, CA 95129

EXAMINER	
VERBRUGGE, KEVIN	

ART UNIT	PAPER NUMBER
2189	

DATE MAILED: 12/20/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/919,361	WOO ET AL.	
	Examiner	Art Unit	
	Kevin Verbrugge	2189	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *04 November 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *25,26,28-35,52,53,55-57 and 59-67* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *25,26,28-35,52,53,55-57 and 59-67* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

This non-final Office action is in response to the amendment filed 11/4/05 which canceled claims 1-21, 24, 38-40, 54, and 58. Claims 25, 26, 28-35, 52, 53, 55-57, and 59-67 remain pending. All objections and rejections not repeated below are withdrawn. The allowance of the pending claims is withdrawn based on the newly located reference found during a pre-allowance updated search. Had the reference been located prior to the previous Office action, the now rejected claims would have been rejected in the previous Office action.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 61, 62, 63, 65, and 66 are rejected under 35 U.S.C. 102(b) as being anticipated by U.S. Patent 5,469,559 to Parks et al.

He shows the claimed memory device in Figs. 1 and 2 as memory controller 12.

He teaches that memory controller 12 receives memory allocation and deallocation notifications from the operating system of CPU 14 at column 3, lines 30-35

and column 4, lines 56-66. He teaches that his memory controller 12 omits refreshing of the memory cells that have been deallocated and refreshes those cells that have been allocated (column 2, line 6 through column 3, line 48 and column 4, line 46 through column 5, line 25).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claim 64 is rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent 5,469,559 to Parks et al.

Parks does not teach that his deallocation notifications are based on virtual memory mapping portions.

However, virtual memory mapping was notoriously well-known at the time of the invention as a common method of memory management, with the operating system using virtual memory to provide the processor with a large address space without having to provide the equivalent amount of physical memory. As various virtual pages are needed, they are mapped in and out of the physical memory, "tricking" the CPU into thinking it has a larger physical memory than it actually does.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to use virtual memory in Parks' device because Parks teaches that his device is useful with any system that has DRAM, and DRAM was the preferred type of memory in virtual memory systems.

****

Claims 25, 26, 29, 30, 31, 52, 53, 55, 56, 59, 60, and 67 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent 5,469,559 to Parks et al. in view of U.S. Patent 6,167,484 to Boyer et al.

Regarding claims 25, 52, 53, 55, 56, 59, 60, and 67, Parks shows the claimed memory as DRAM subsystem 20 in Figs. 1 and 2.

He shows the claimed memory controller as memory controller 12.

He teaches that memory controller 12 receives memory allocation and deallocation notifications from the operating system of CPU 14 at column 3, lines 30-35 and column 4, lines 56-66. He teaches that his memory controller 12 omits refreshing of the memory cells that have been deallocated and refreshes those cells that have been allocated (column 2, line 6 through column 3, line 48 and column 4, line 46 through column 5, line 25).

Parks does not teach that his deallocation notifications are based on virtual memory mapping portions.

However, virtual memory mapping was notoriously well-known at the time of the invention as a common method of memory management, with the operating system using virtual memory to provide the processor with a large address space without having to provide the equivalent amount of physical memory. As various virtual pages are needed, they are mapped in and out of the physical memory, "tricking" the CPU into thinking it has a larger physical memory than it actually does.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to use virtual memory in Parks' device because Parks teaches that his device is useful with any system that has DRAM, and DRAM was the preferred type of memory in virtual memory systems.

Parks does not teach the claimed recent-access flags or keeping track of which cells have been accessed in a manner that refreshed the memory cells during a previous refresh cycle interval and omitting refreshing of those cells that have been accessed in a previous refresh cycle interval.

However, Boyer teaches just such a limitation. Specifically, he shows tile history qualifiers 808a, 808b, ... 808N. These qualifiers correspond to groups of one or more memory cells, as claimed, and indicate whether the corresponding groups of memory cells are in use (column 5, lines 11-14, column 8, lines 1-3, column 14, line 48 through column 15, line 36, column 24, lines 40-43, column 25, line 50 through column 26, line 25). Boyer's refresh logic omits refreshing of memory cells that are not in use (column 5, lines 14-19, column 7, lines 46-51).

Boyer's history qualifiers anticipate the claimed recent-access flags and keep track of which memory cells have been recently accessed, since his history qualifiers are "processed whereby refreshing is not performed on a row of cells that do not need refreshing (i.e., rows that are inactive, or rows that were recently read or written since these accesses inherently do a refresh of the rows)" (emphasis added, column 5, lines 16-19). Boyer clearly teaches that one of the key advantages of his device is keeping track of reads and writes with his history qualifier bits so that memory locations which have recently been read or written (which inherently performs a refresh of the accessed location) are not needlessly refreshed soon after, wasting power and processing time and bandwidth (column 3, lines 22-28). Other passages addressing this key advantage of his device include column 7, lines 12-18 and 46-51, column 14, lines 38-48, and column 23, lines 3-8.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to include Boyer's tile history qualifiers in Parks' device to save additional power. Parks teaches that his device keeps track of which parts of memory are in use and doesn't refresh those that are not in use, saving power by not refreshing areas not in use. Boyer's device goes one step further, not refreshing areas that are in use and were recently refreshed due to a read or write.

Regarding claim 26, both Parks and Boyer disclose DRAM and omitting refreshing to save power.

Regarding claims 29 and 30, Parks shows the claimed use bits as the region descriptor bits stored in SRAM 208 in Fig. 2 and described at column 2, line 60 through column 3, line 13.

Regarding claim 31, Boyer shows a plurality of discrete memory devices in Fig. 8 as memory array tiles 802, for example, and teaches that his use bits are on the memory devices in Fig. 2, for example. Including multiple memory devices in Parks' system and putting the use bits in the memory devices of Parks' system would have been obvious to one of ordinary skill in the art at the time the invention was made to achieve the advantages presented by those design choices as shown by Boyer. Having more memory devices increases the amount of data storage capacity. Placing the bits on the memory devices simplifies memory controller construction, among other things.

****

Claims 32, 34, 35, and 57 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent 5,469,559 to Parks et al. in view of "Optimizing the DRAM Refresh Count for Merged DRAM/Logic LSIs" by Ohsawa et al.

Regarding claims 32 and 57, Parks does not disclose a cache in his memory controller.

Ohsawa mentions the claimed caching of memory rows and not refreshing those rows at section 3.2.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to include a cache in Parks' memory controller for the improved operation speed provided by a cache as known in the art at the time of the invention.

In section 3.2, Ohsawa clearly teaches not refreshing data in DRAM if that data is out of date with its replacement data in a cache. In other words, Ohsawa teaches not refreshing a location in DRAM if "dirty" data in the cache will eventually overwrite it.

Ohsawa does not teach omitting refreshing of rows that are not dirty in the cache (have not been written to).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to mark every cache entry dirty in the cache whether it had been written to or not, to maximize power savings. Then, whenever any entry was copied from DRAM to the cache, the use bit of that entry in DRAM would be marked as out of use and no longer refreshed, saving power. Then, even if the data was only read from the cache and never written to, it would be marked as dirty and therefore would eventually be flushed back to DRAM, at which time its use bit would be set to indicate that it should be refreshed from then on. This minor modification of Ohsawa would have been obvious to one of ordinary skill in the art who was concerned with maximizing power savings as Ohsawa and Parks are.

Regarding claims 34 and 35, Parks uses region descriptor bits in SRAM 208 as discussed above.

****

Claims 28 and 33 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent 5,469,559 to Parks et al. in view of U.S. Patent 6,167,484 to Boyer et al., further in view of "Optimizing the DRAM Refresh Count for Merged DRAM/Logic LSIs" by Ohsawa et al.

Regarding claim 28, neither Parks nor Boyer discloses a cache in their memory controller.

Ohsawa mentions the claimed caching of memory rows and not refreshing those rows at section 3.2.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to include a cache in Parks' memory controller for the improved operation speed provided by a cache as known in the art at the time of the invention. Furthermore, as taught by Ohsawa, data that is cached in the memory controller need not be refreshed in the memory as long as it is eventually written back to the memory. This provides the additional power savings of not having to refresh the data that is cached.

Regarding claim 33, Parks and Ohsawa do not teach omitting refreshing of recently accessed rows.

Boyer shows the claimed operation using recent-access flags (history qualifiers) as discussed above.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to include Boyer's recent-access flag operation to further reduce the amount of power consumed by Parks' device since Boyer teaches that his recent-access flags help reduce power even further by not refreshing rows that were recently accessed.

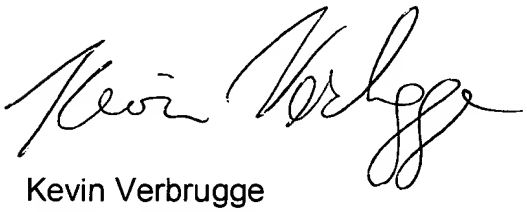
Conclusion

Any inquiry concerning this Office action should be directed to the Examiner by phone at (571) 272-4214.

Any response to this Office action should be labeled appropriately (including serial number, Art Unit 2189, and type of response) and mailed to Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, hand-carried or delivered to the Customer Service Window at the Randolph Building, 401 Dulany Street, Alexandria, VA 22313, or faxed to (571) 273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only.

For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197.



Kevin Verbrugge
Primary Examiner
Art Unit 2189